Application Note | March 1998 | AN9798

Description and Use of the Evaluation Board

The HI3304 is a 25 MSPS, 4-bit analog-to-digital converter. It obtains its high speed operability by implementing a sequential parallel conversion technique. One clock cycle is required for each conversion. This is achieved by having two phases during the conversion process, the “Auto Balance” phase during the low period of the clock and the “Sample Unknown” phase during the high period of the cycle. For a complete technical discussion of the architecture and timing of the converter, please refer to the HI3304 data sheet, available in the Data Acquisition Products Data Book or it can be found on the world wide web at www.intersil.com.

The HI3304 evaluation board includes a number of features which allow easy use in the lab while providing added versatility. The evaluation board includes an HA5033 unity gain buffer amplifier which is to be used as an input driver. It can be removed from the signal path or even from the board if it is not needed. A prototyping area is provided on the board for the addition of circuitry such as a voltage reference or alternate input driver. All input/output functions of the HI3304 are accessible either through a 50 pin edge connect or BNC connectors.

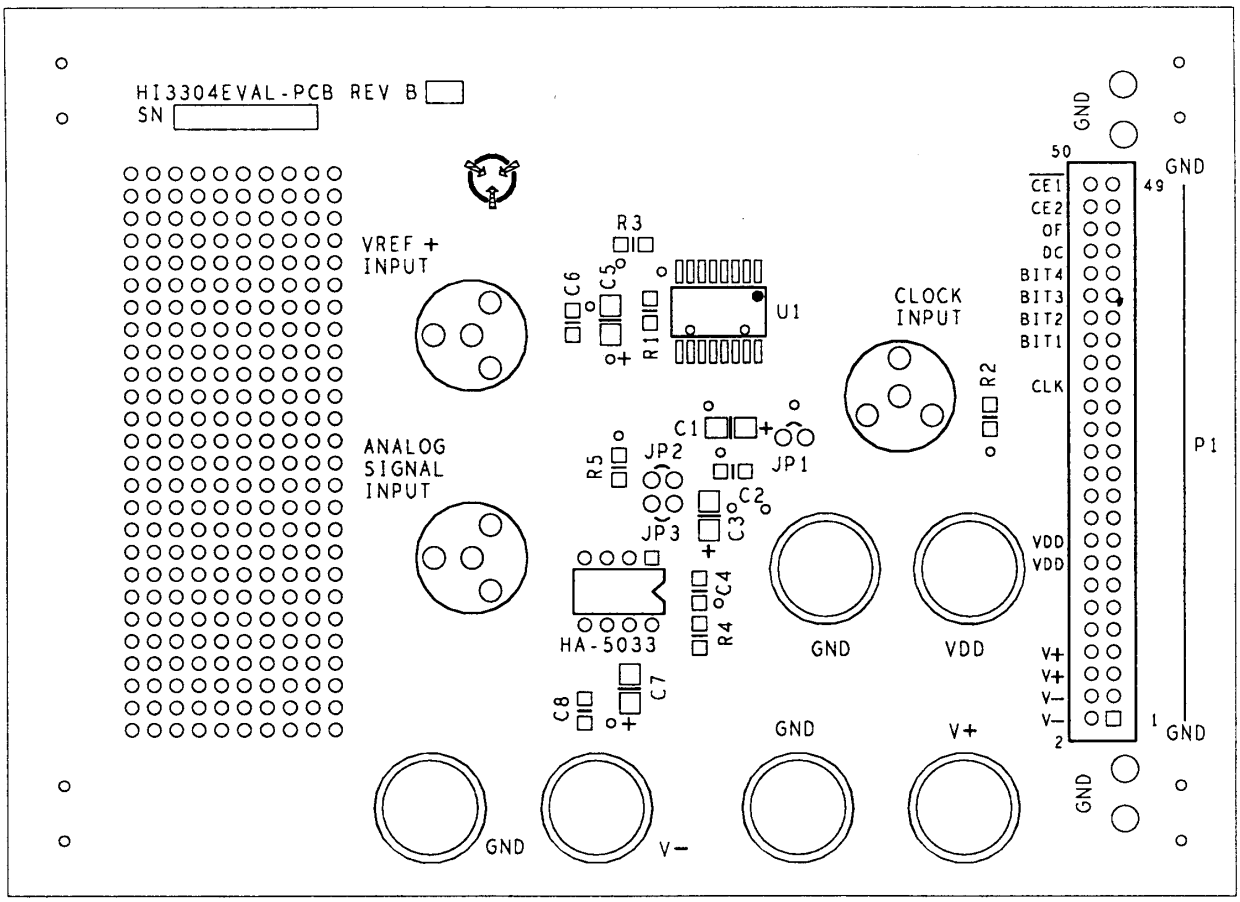


FIGURE 1. HI3304 EVALUATION BOARD (1X SIZE)

Evaluation Board Connections

External supplies and signal sources needed to operate the board:

1. +5V for HI3304 V_{DD}.
2. 0 to 5V, 50% duty cycle, 25MHz square wave for HI3304 CLK.
3. +2V for HI3304 $V_{REF}+$.
4. ±12V for optional HA5033 analog input buffer.
5. Analog input signal (0 to 2V range).
6. To capture the data at the output, some type of DAS (Data Acquisition System) will be needed, or the user can choose to use a higher resolution DAC and view the output on a spectrum analyzer or oscilloscope.

The HI3304 is provided in SOIC form. A PDIP package is also available, but no evaluation board is available to support that package.

Power is supplied to the HI3304 using the banana jacks or the 2 edge connector pins labeled V_{DD}. The ground connection can be made either through the GND banana jacks or the edge connector pins labeled GND. For convenience, all of the pins on the right hand side of the edge connector are tied to the ground plane. The clock signal is connected to the BNC labeled CLOCK INPUT which is terminated with a 50Ω resistor, R_2. The 2V reference is supplied through a BNC labeled $V_{REF}+$ INPUT.

The input control pin $\overline{CE1}$ is tied by a 50Ω resistor to ground. The input control pin CE2 is tied by a 50Ω resistor to V_{DD}. Both of these pins are accessible through the edge connector. $V_{REF}-$ (pin 13) is jumpered to ground which is the most common use of this pin. Jumper J_1 can be removed if $V_{REF}-$ is to be actively driven. This provides access to pin 13 of the converter via the jumper stem or the solder hole directly.

The analog input V_{IN} (pin 11) can be driven directly from the BNC connector labeled ANALOG SIGNAL INPUT or from the included HA5033 buffer amplifier. To select the HA5033 input option, install Jumper J_3 and make sure that Jumper 2 is not installed. If jumper J_2 is selected and J_3 removed, then the HA5033 is bypassed and the input is driven from the BNC.

The HA5033 is powered by +12V connected to the V+ banana jack and by -12V connected to the V- banana jack. The supplies can also be connected through the edge connector pins V+ and V-. All supply decoupling caps are included on the board.

The HI3304 digital output bits, BIT 1 through BIT 4, the overflow bit, OF, and the data change bit, DC, are all accessible through their respective pins on the edge connector. In addition, the left side of the board contains an array of solder holes intended for use as a prototyping area.

Power Up/Down Sequence

The correct power up sequence for the evaluation board is:

1. Power up the HI3304 5V supply.
2. Power up the HI3304 2V reference voltage.
3. Enable the HI3304 clock waveform.
4. Power up the HA5033 ±12V supplies.
5. Enable the analog input.

The power down sequence is the reverse of the power up sequence:

1. Disable the analog input.
2. Power down the HA5033 ±12V supplies.
3. Disable the HI3304 clock waveform.
4. Power down the HI3304 2V reference voltage.
5. Power down the HI3304 5V supply.

Board Test

To determine if the eval board is functioning properly, perform the following test:

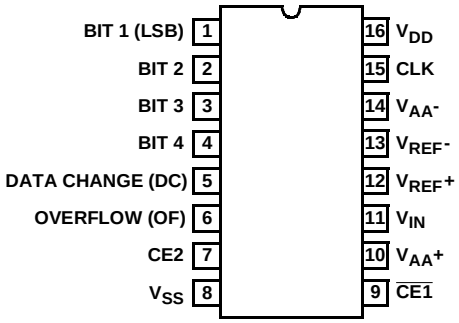
1. Drive the clock with a 25MHz square wave that has an amplitude swing of approximately $2V_{P-P}$ from +1V to +3V.
2. Drive the analog input with a 5MHz sinewave that has an amplitude of $2V_{P-P}$, centered around +1V DC offset.
3. Use either JP2 or JP3, but not both. JP2 will give you direct input to the DUT, whereas JP3 will give you an op amp buffered input.
4. Using a DAS (Data Acquisition System) that is capable of 4 bits and can operate at 25MHz, capture the data and perform an FFT on it. Calculate ENOB.
5. If ENOB is greater than 3.5 bits, the board and part are probably functioning properly. If ENOB is not greater than 3.5 bits, then vary the +1V offset and the amplitude of the input sinewave and see if that makes ENOB higher. The optimum input level would be centered perfectly and operating just below the $2V_{P-P}$ swing amplitude to insure that all or most of the codes were being used. Check to make sure that the converter is not clipping positive, negative, or both.
6. Alternate test method: Obtain a higher resolution DAC and use that to reconstruct the ADC's output. Compare the reconstructed signal to the input and check for amplitude, missing codes, and frequency. Keep in mind that the reconstructed signal will be quantized, or stair-stepped.

General Comments

The HI3304 can be pushed to its limits by varying the clock frequencies and duty cycle, with degradation in performance occurring as 35 MSPS is exceeded. For slower sampling rates, reductions in power supply current can be realized by changing the clock duty cycle such that the auto-balance time is reduced (see data sheet for explanation of 'auto-balance'). An external flip-flop or latch is not needed. The output drivers are designed to drive bus lines directly.

For more information on the HI3304 ADC, please refer to the data sheet or call 1-888-INTERSIL or 321-724-7143.

Pinout



Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION	
1	Bit 1	Bit 1 (LSB).	Output Data Bits (High = True)
2	Bit 2	Bit 2.	
3	Bit 3	Bit 3.	
4	Bit 4	Bit 4 (MSB).	
5	DC	Data Change.	
6	OF	Overflow.	
7	CE2	Three-State Output Enable Input, active low. See the Chip Enable Truth Table.	
8	V_{SS}	Digital Ground.	
9	$\overline{CE1}$	Three-State Output Enable Input, active high. See the Chip Enable Truth Table.	
10	V_{AA}+	Analog Power Supply, +5V.	
11	V_{IN}	Analog Signal Input.	
12	V_{REF}+	Reference Voltage Positive Input.	
13	V_{REF}-	Reference Voltage Negative Input.	
14	V_{AA}-	Analog Ground.	
15	CLK	Clock Input.	
16	V_{DD}	Digital Power Supply, +5V.	

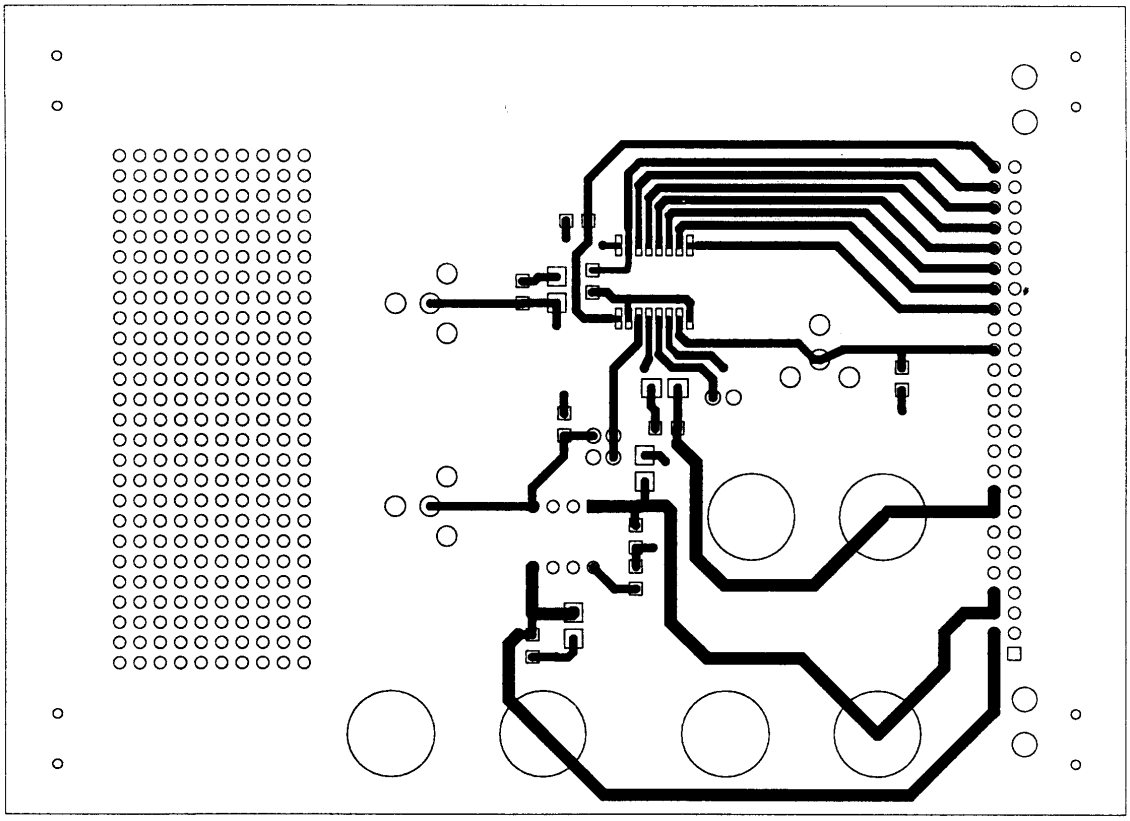


FIGURE 2. COMPONENT SIDE OF EVALUATION BOARD (1X SIZE)

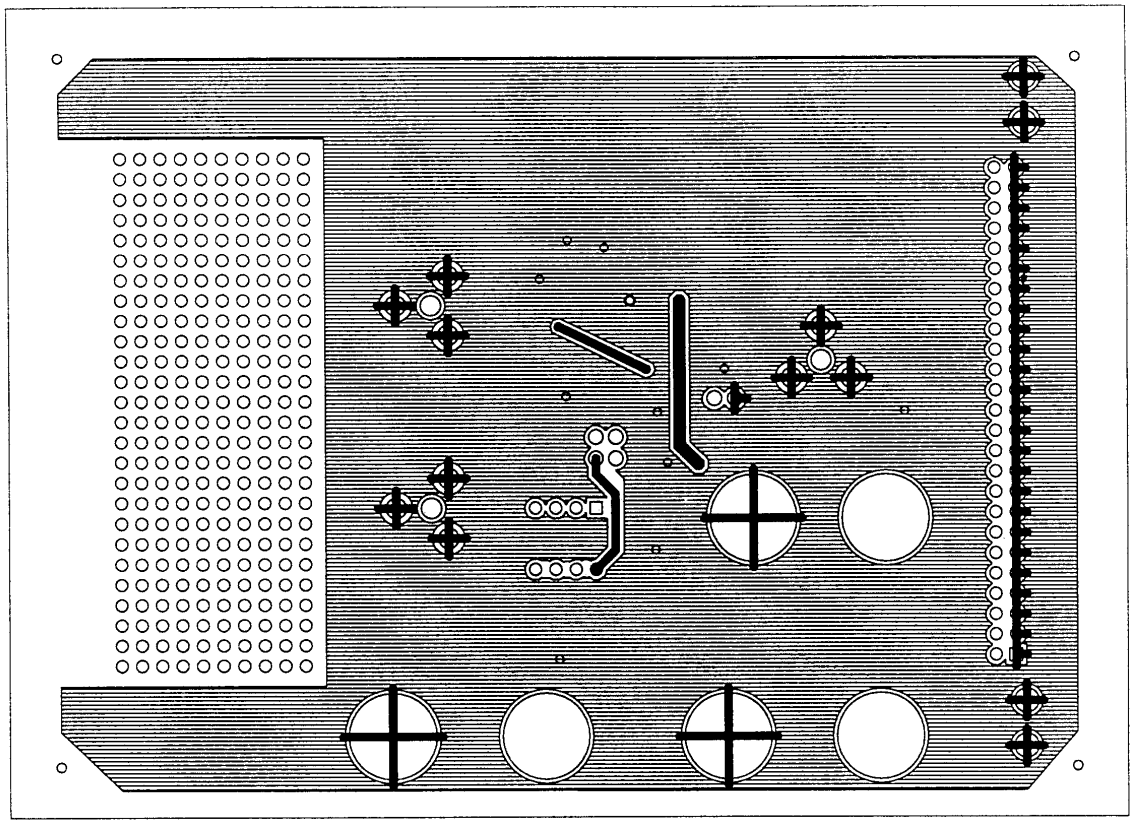
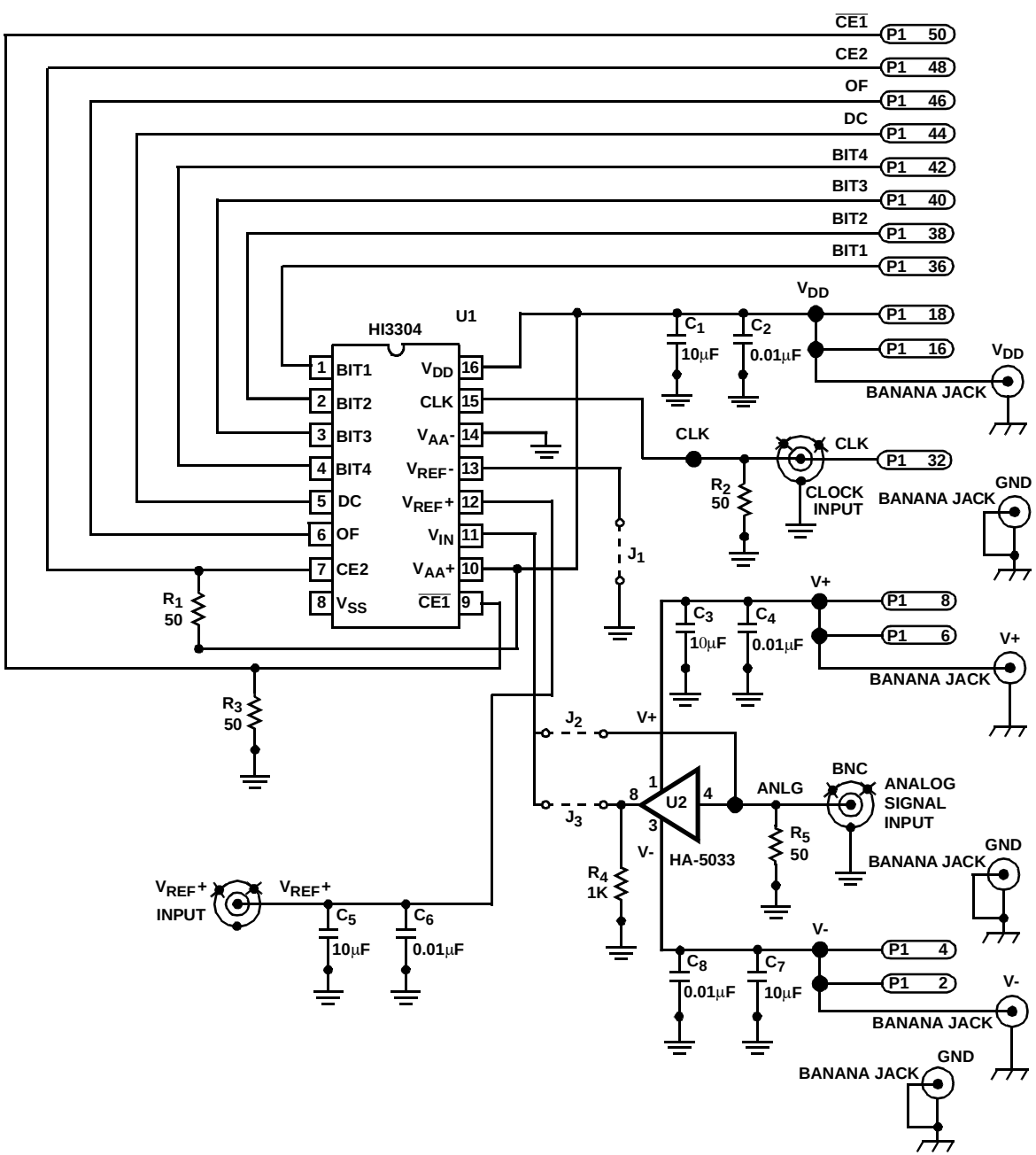
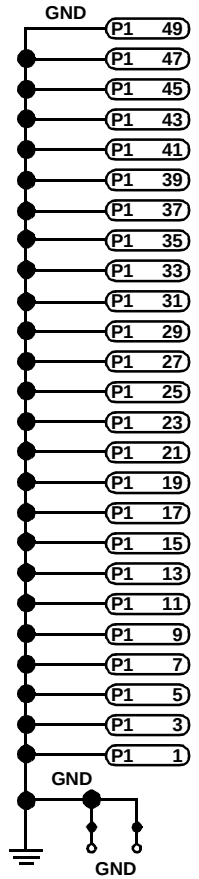
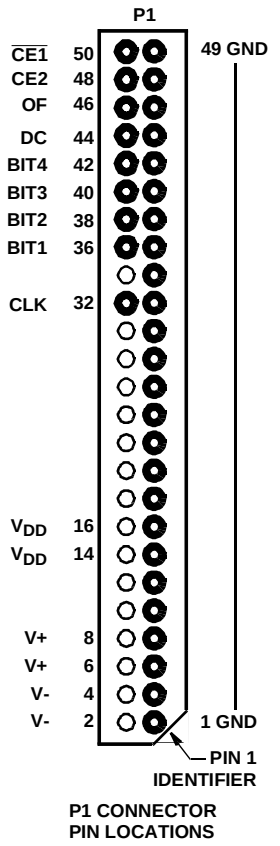


FIGURE 3. BACK SIDE OF EVALUATION BOARD (1X SIZE)







P1 CONNECTOR PIN LOCATIONS

Parts List

Capacitors

C_2, C_4, C_6, C_8 = 0.01µF Ceramic, 10%, 1206, 10V
C_1, C_3, C_5, C_7 = 10µF Tantalum, 10%, CASE B, 10V

Resistors

R_1-R_3, R_5 = 49.9Ω, 1%, 1206, 1/8W
R_5 = 1000Ω, 1%, 1206, 1/8W

ICs

U1 = HI3304 (HI3304JIB, 16 Ld SOIC)
U2 = HA5033 (HA3-5033-5, 8 Ld PDIP)

Connectors

P1 = Terminal Strip 50 Pin; 0.025 sq. pins; 0.100 centers
Six BNCs = AMP 221123-3 PCB mount BNC;
Six Standard Banana Jacks